REMARKS/ARGUMENTS

In response to the Office Action mailed April 19, 2005, applicant respectfully requests reconsideration. In the Office Action, claims 1-15 were rejected. By this response, applicant has amended the Specification to correct minor editorial matters. Claim 11 has been amended and new claims 16-18 have been added. Accordingly, claims 1-18 are currently pending in this application.

Claim Rejection Under 35 U.S.C. §102

Claims 1-15 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,489,574 to Otaki et al. ("Otaki"). This rejection is respectfully traversed, as Otaki does not teach every element of claim 1, as is required for a proper rejection under 35 U.S.C. §102(b).

Independent claim 1 recites a method comprising:

A. providing a substrate having a first surface and a second surface, the first surface being adapted for mounting an electronic device thereon, the substrate including a grid of electrically conductive vias extending from a region proximate the first surface to a region proximate the second surface, each via being one of a signal via, a ground via and a power via;

B. removing at least one of the vias to form a void between at least one ground via and at least one power via; and

C. connecting each of the at least one ground via proximate the void to one of the at least one power vias proximate the void with a filter device proximate the second surface of the substrate.

Otaki teaches a printed wiring board device having multiple terminals arranged in a matrix, including signal connection holes, signal lines and lands divided into plural blocks. The invention involves drawing out the wiring patterns of the signal lines regularly from many lands formed in the matrix on the assembling surface of the grid array type package to make it easier for the printed wiring board to effectuate wiring

connections without making them complicated or increasing the number of layers of the printed wiring board. Furthermore, the invention provides ground patterns that surround the signal lines to reduce radiant noises (see the Abstract). As shown in Fig. 3, the capacitor 104 is connected between the power supply terminal 108 and the ground terminal 109.

Otaki does not teach the invention recited in independent claim 1. Specifically, Otaki does not teach removing at least one of the vias to form a void between at least one ground via and at least one power via. Otaki teaches a double-layer printed wiring board having a pattern of lands 1 and through-holes 3, 5 and 7 (Figs. 1 and 2, Col. 5, lines 7-14). There is no teaching or suggestion in Otaki of removing vias, and no teaching or suggestion of removing vias (or through holes) to form a void between at least one ground via and at least one power via.

Furthermore, Otaki does not teach connecting each of the at least one ground via proximate the void to one of the at least one power vias proximate the void with a filter device proximate the second surface of the substrate. First, because Otaki does not teach or suggest forming a void between at least one ground via and at least one power via, Otaki cannot teach connecting power and ground vias with a filter device proximate the void. Second, Otaki does not teach connecting power and ground vias with a filter device proximate the void proximate the second surface of the substrate. The bypass capacitor shown in Fig. 3 of Otaki connects a power supply terminal on one side of the board to a ground terminal on the opposite side of the board.

Accordingly, since Otaki does not teach every element recited in independent claim 1, the rejection of independent claim 1 under 35 U.S.C. §102(b) is improper and should be withdrawn.

Claims 2-5 depend from independent claim 1 and are allowable for at least the same reasons as independent claim 1.

Independent claim 6 recites a method comprising:

A. providing a substrate having a first surface and a second surface, the first surface being adapted for mounting an electronic device thereon;

B. forming a grid of electrically conductive vias extending from a region proximate the first surface to a region proximate the second surface, each via being one of a signal via, a ground via and a power via;

C. removing at least one of the vias to form a void between at least one ground via and at least one power via; and

D. connecting each of the at least one ground via proximate the void to one of the at least one power vias proximate the void with a filter device proximate the second surface of the substrate.

Applicant asserts that Otaki does not teach the invention recited in independent claim 6. As described above, Otaki does not teach removing at least one of the vias to form a void between at least one ground via and at least one power via. Otaki teaches a double-layer printed wiring board having a pattern of lands 1 and through-holes 3, 5 and 7 (Figs. 1 and 2, Col. 5, lines 7-14). There is no teaching or suggestion in Otaki of removing vias, and no teaching or suggestion of removing vias to form a void between at least one ground via and at least one power via.

Furthermore, Otaki does not teach connecting each of the at least one ground via proximate the void to one of the at least one power vias proximate the void with a filter device proximate the second surface of the substrate. First, because Otaki does not teach or suggest forming a void between at least one ground via and at least one power via, Otaki cannot teach connecting power and ground vias with a filter device proximate the void. Second, Otaki does not teach connecting power and ground vias with a filter device proximate the void proximate the second surface of the substrate. The bypass capacitor shown in Fig. 3 of Otaki connects a power supply terminal on one side of the board to a ground terminal on the opposite side of the board.

Accordingly, since Otaki does not teach every element recited in independent claim 6, the rejection of independent claim 6 under 35 U.S.C. §102(b) is improper and should be withdrawn.

Claims 7-10 depend from independent claim 6 and are allowable for at least the same reasons as independent claim 6.

Independent claim 11 recites a method comprising:

A. providing a substrate having a first surface and a second surface, the first surface being adapted for mounting an electronic device thereon;

B. forming a grid including a plurality of electrically conductive vias extending from a region proximate the first surface to a region proximate the second surface, each via being one of a signal via, a ground via and a power via, and a void between at least one ground via and at least one power via, the void being an area lacking at least one via; and

C. connecting one of the at least one ground vias proximate the void to at least one of the at least one power vias proximate the void with a filter device proximate the second surface of the substrate.

Applicant asserts that Otaki does not teach the invention recited in independent claim 11. Otaki does not teach forming a grid including a plurality of electrically conductive vias extending from a region proximate the first surface to a region proximate the second surface, each via being one of a signal via, a ground via and a power via, and a void between at least one ground via and at least one power via, the void being an area lacking at least one via. Otaki teaches a double-layer printed wiring board having a pattern of lands 1 and through-holes 3, 5 and 7 (Figs. 1 and 2, Col. 5, lines 7-14). There is no teaching or suggestion in Otaki of forming a void between at least one ground via and at least one power via.

Furthermore, Otaki does not teach connecting each of the at least one ground via proximate the void to one of the at least one power vias proximate the void with a filter device proximate the second surface of the substrate. First, because Otaki does not teach or suggest a void between at least one ground via and at least one power via, Otaki cannot teach connecting power and ground vias with a filter device proximate the void. Second, Otaki does not teach connecting power and ground vias with a filter device proximate the void proximate the second surface of the substrate. The bypass capacitor shown in Fig. 3 of Otaki connects a power supply terminal on one side of the board to a ground terminal on the opposite side of the board.

Accordingly, since Otaki does not teach every element recited in independent claim 11, the rejection of independent claim 11 under 35 U.S.C. §102(b) is improper and should be withdrawn.

Claims 11-15 depend from independent claim 11 and are allowable for at least the same reasons as independent claim 11.

New Claims 16-18

New claims 16-18 have been added to further define the applicant's contribution to the art. No new matter has been added.

Amendment to the Specification

Applicant has amended the Specification to correct typographical errors. No new matter has been added.

Based on the foregoing amendments and remarks, applicant asserts that pending claims 1-18 are allowable over the prior art of record and respectfully requests that a timely Notice of Allowance be issued in this application.

In the event the Examiner deems personal contact desirable in the disposition of this case, the Examiner is invited to call the undersigned attorney at 508.293.7835.

Please charge all fees occasioned by this submission to Deposit Account No. 05-0889.

Respectfully submitted,

5/10/05

Date

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